MAJOR RESEARCH PROJECT

Title

"On Chip 3D Simulator for Network-on-Chip(NoC)"

Final report submitted

to

University Grants Commission
Bahadur Shah ZafarMarg
New Delhi – 110 002
2011-2013

by

Principal Investigator
Prof. ABDUL QUAIYUM ANSARI
Professor
Department of Electrical Engineering
Jamia Millia Islamia (A Central University)
New Delhi – 110 025

Annexure — IX

UNIVERSITY GRANTS COMMISSION
BAHADUR SHAH ZAFAR MARG
NEW DELHI – 110 002

PROFORMA FOR SUBMISSION OF INFORMATION AT THE TIME OF SENDING THE FINAL REPORT OF THE WORK DONE ON THE PROJECT

1. NAME AND ADDRESS OF THE PRINCIPAL INVESTIGATOR:

ABDUL QUAIYUM ANSARI
Address: Residence
63-T, Sector - 8, DDA - SFS Flats
JasolaVihar, New Delhi-110025
Phone. +91-11-29946605

2. NAME AND ADDRESS OF THE INSTITUTION:

Department of Electrical Engineering
Jamia Millia Islamia
New Delhi – 110 025

3. UGC APPROVAL LETTER NO. AND DATE: F. No.39-895/2010(SR) Dated 13/01/2011

4. DATE OF IMPLEMENTATION: 01/02/2011

5. TENURE OF THE PROJECT: 2 years

6. TOTAL GRANT ALLOCATED: Rs.8,94,000/-(Rupees Eight Lakh Ninety Four Thousand)

7. TOTAL GRANT RECEIVED: Rs. 6,99,000/- (Rupees Six Lakh Ninety Nine Thousand)

8. FINAL EXPENDITURE: Rs. 5,56,267/- (Rupees Five Lakh Fifty Six Thousand Two Hundred Sixty Seven)

9. TITLE OF THE PROJECT: "On Chip 3D Simulator for Network-on-Chip (NoC)"

10. OBJECTIVES OF THE PROJECT:

The objectives of the proposed project are as following(s):

1. To study the various network topology
2. To study the various types routing strategy
3. To build a simulator based on the hardware and software co-design approach

11. WHETHER OBJECTIVES WERE ACHIEVED

The Network-on-Chip (NoC) represents a new communication paradigm for increasingly complex on-chip networks. The NoC provides technique for generic on-chip interconnection network realized by routers that connects processing elements (PE) like ASICs, FPGAs, memories, IP cores etc. The NoC offers flexibility, scalability, predictability, and higher bandwidth, low latency and provision for concurrent communications. The scales in VLSI technology to deep sub-micron (DSM) have started integrating large number of processing elements into silicon. The existing shared bus based communications are not able to achieve the required latency. This has raised the requirement of good communication architecture and topology in 3-D space. The future System-on-Chip (SoC) will contain billions of transistors, composing hundreds to 1000 of IP cores.

The principle objective of the project was to propose and simulate an efficient, fast, and dynamic technique for allocation and de-allocation of virtual channel in 3-D Network-on-Chip.

Another object of the invention is to provide a circular First in, First out (FIFO) that is can read and write in general, particularly can allocate and de-allocate the virtual channels simultaneously.

Yet another objective was to provide a reservation policy for allocation of virtual channel. The reservation policy guarantees that one virtual channel would be reserved for every physical channel.

Still another objective of the invention was to dispense and release multiple virtual channels simultaneously.

The entire objective which was set in the beginning was met.

12. ACHIEVEMENTS FROM THE PROJECT:

We have been able to produce two patents (applied), published books and papers in various refereed journals and conferences.

Patents:

1. A. Q. Ansari, M. A. Khan, "Parallel and Dynamic Virtual Channel Manager (VCM) for 3-D Network-On-Chip (NoC) Router", *Indian Patent JOURNAL.*
   Submitted: 03/08/2011 16:07:38.

2. A. Q. Ansari, M Ayoub Khan, "Architecture of 3-D Network-On-Chip (NoC) Router with Guided Flit Logic", *filed with Indian Patent office*, New Delhi.
   Submitted: 18/01/2013 15:39:18.

Books Written/ Books Edited:

1. M Ayoub Khan, A. Q. Ansari, "Efficient Topologies for 3-D Network-on-Chip", Multicore Technology Architecture, Reconfiguration, and Modelling Publisher: CRC Press (Taylor and Francis) U.K., 2013, ISBN-13: 9781439880630).

Journals Edited:

1. M Ayoub Khan, A. Q. Ansari, Special Issue on "Emerging Trends in on-Chip Communicaitons," International Journal of Embedded and Real Time System (IJRTES),IGI Global, UK, ISSN (Online): 1741-1076 - ISSN (Print): 1741-1068, IEEE WICT 2011

Magazine/Newsletter Publications:

1. M Ayoub Khan, A Q Ansari, "*A Journey from Computer Networks to Networks-on-Chip*". IEEE Beacon, Vol. 31, No. 1, pp. 71-77, March 2012.

2. Sapna Tyagi, Preeti Sirohi A Q Ansari, M Y khan, M Ayoub Khan, "*e-Learning : Re-emerging paradigm for enhanced learning*", IEEE Learning Technology Newsletter Vol. 13, Issue 4, October 2011.

Paper published in International Refereed Journals and in the proceedings of Conferences:

1. M Ayoub Khan, **A Q Ansari**, "High-Speed Dynamic TDMA Arbiter for Inter-Layer Communications in 3-D Network-on-Chip", *Journal of High Speed Networks, IOS Press*, Netherlands, Vol. 18(3), pp.141-155, **2012**. DOI 10.3233/JHS-2012-0448,ISI Indexed.
2. M. A. Khan, **A. Q. Ansari**, "Area-Efficient Programmable Arbiter for Inter-Layer Communications in 3-D Network-on-Chip," *Central European Journal of Computer Science*, Springer, Vol. 2, Issue 1, pp 76-85, March **2012**.

3. M. A. Khan, **A. Q. Ansari**, "Modelling and Simulation of 128-Bit Crossbar switch for Network-on-Chip", *International Journal of VLSI and Communications System, AIRCC,*Australia, Vol. 2, No. 3, pp. 213 – 222, September **2011**. ISSN: 0976 – 1527, DOI:10.5121/vlsic.2011.2318.
4. M. A. Khan, **A. Q. Ansari**, "An Quadrant-XYZ Routing Algorithm for 3-D Asymmetric Torus Network-on-Chip," *International Journal ofACM Jordan,* Vol. 2, No. 2, pp. 18 – 26, June **2011**.
5. M. A. Khan, **A. Q. Ansari**, "An Efficient Tree-Based Topology for Network-on-Chip," *Proc. World Congress on Information and Communication Technology* (WICT 2012), Mumbai, pp. 1316 – 1321, Dec. **2011**. [Online] Available: www.ieeexplore.org DOI: 10.1109/WICT.2011.6141439
6. M. A. Khan, **A. Q. Ansari**, "n-Bit Multiple Read abd Write FIFO Memory Model for Network-on-Chip," *Proc. World Congress on Information and Communication Technology* (WICT 2012), Mumbai, pp. 1322 – 1327, Dec. **2011**. [Online] Available: www.ieeexplore.org DOI: 10.1109/WICT.2011.6141440
7. M. A. Khan, **A. Q. Ansari**, "Design of 8-Bit Programmable Crossbar Switch for Network-on-Chip Router," *Int. Workshop on VLSI*, Chennai, **Springer-Verlag Berlin Heidelberg**, CCIS 197, Lecture Notes in *Trends in Network and Communication*, D.C. Wyld et al. (Eds.), pp. 526 – 535, July 2011.
8. M Ayoub Khan, **A. Q. Ansari** , "From Computer Networks to Network-on-Chip", *International Conference on Nanoscience, Engineering, and Advanced Computing*, July, 8-10, 2011, AP, India, pp. 28-33.
9. M. A. Khan, **A. Q. Ansari**, "Quadrant-Based XYZ Dimension Order Routing Algorithm for 3-D Asymmetric Torus Routing Chip," *Proc. International Conference on Emerging Trends in Networks and Computer Communications,* (ETNCC 2011), Udaipur, India, pp. 121 – 124, April 22 – 24, 2011. [Online] Available: www.ieeexplore.org, DOI: 10.1109/ETNCC.2011.5958499
10. M. A. Khan, **A. Q. Ansari** , "Low-Power Architecture for dTDMA Transmitter and Receiver for Vertical BUS", Proc. IEEE International Conference on Emerging Trends in Networks and Computer Communications, April 22-24, 2011, Udaipur, India pp. 350 – 354, IEEE Catalogue Number: CFP1196N-CDR, ISBN: 978-1-4577-0238-9.
11. M. A. Khan, **A. Q. Ansari**, "128-Bit High-Speed FIFO Design for Network-on-Chip," *Proc.* IEEE *International Conference on Emerging Trends in Computing* (ICETC 2011), Coimbatore, pp. 116 – 121, March 17 - 18, 2011.
12. M. A. Khan, **A Q Ansari**, "A Review of Hyper-Torus based Topologies for Network-on-Chip", *Proc.* IEEE *International Conference on Emerging Trends in Computing* (ICETC 2011), Coimbatore, pp. 109 – 115, March 17 - 18, 2011.

13. SUMMARY OF THE FINDINGS:

The present investigation provides an improved technique for allocation and de-allocation of virtual channel in 3-D Network-on-Chip. The VC allocator in Virtual Channel Manager allocates a virtual channel when a head flit of a packet is received at the port. After allocating a free VC to a packet the necessary entry in Lookup Table (LUT) is updated. The entry in

LUT contains information about virtual channel as VC ID, physical port ID, packet ID. When a TAIL flit is received then the process of automatic de-allocation is triggered. Thus the invention has a provision of automatic allocation and de-allocation of Virtual Channel based on flit type. We also proposed an efficient routing algorithm for 3-D NoC routing.

14. CONTRIBUTION TO THE SOCIETY:

The contribution to the scientific society is in the terms of new techniques for virtual channels, routing and 3-D NoC infrastructure management. One Ph. D has been produced in the area of Network-on-Chip. Now, other students are also start working in this area. Also, we have created a state-of-art in the area of Network-on-Chip.

15. WHETHER ANY Ph. D. ENROLLED/PRODUCED OUT OF THE PROJECT:

Produced: Dr. Mohamad Ayoub Khan

Enrolled: Mohammad Rashid Ansari

16. NO. OF PUBLICATIONS OUT OF THE PROJECT:

No. of Patents: 2

No. of Books Written/ Books Edited / Journals Edited: 2

Magazine/Newsletter Publications: 2

No. of paper published in International Refereed Journals and in the proceedings of Conferences: 12 (Papers Attached)

12/3/2014

(PRINCIPAL INVESTIGATOR)

Prof. A. Q. ANSARI

Prof. ABDUL QUAIYUM ANSARI
Department of Electrical Engineering
Faculty of Engg. and Technology
Jamia Millia Islamia
New Delhi 110025

20/03/14

for **(REGISTRAR /PRINCIPAL)**

Registrar
Jamia Millia Islamia
(A Central University)
New Delhi-110025